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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,340	10/17/2003	Slawomir K. Ilnicki	10031168-1	9443

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AGILENT TECHNOLOGIES, INC.
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EXAMINER	
CHOU, ALBERT T	
ART UNIT	**PAPER NUMBER**
2616	

MAIL DATE	DELIVERY MODE
05/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/688,340	ILNICKI ET AL.	
	Examiner	Art Unit	
	Albert T. Chou	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-11* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 6-11 are rejected under 35 U.S.C. 102(e) as being unpatentable over US Patent No. 7,111,208 to Hoang et al. (hereinafter "Hoang").

Regarding claim 1, Hoang teaches an apparatus comprising:

a deserializer **[Fig. 3; CDR & Deserializer/Transmit Block 310]** converting a serial high bandwidth channel from a serial datastream to an output high bandwidth parallel datastream;

memory holding an extra packet **[Fig. 3; Elastic FIFO 401/Transmit Block 310; col. 4, lines 48-65]** for the low-bandwidth channel,

memory **[Fig. 3; Lane Alignment FIFO 308/Transmit Block 310]** holding the high bandwidth parallel datastream while the packet for the low-bandwidth channel is being sent **[Fig. 3; Management & Control Block 330, Elastic FIFO 401/Transmit Block 310; namely, no frequency difference between a recovered clock and a**

local reference clock and thus no insertion or deletion of bytes are required; col. 4, lines 48-65];

a serializer **[Fig. 3; CMU & Serializer/Transmit Block 310]** converting a parallel datastream to a serial datastream; and

control logic **[Fig. 3; Management & Control Block 330]** accepting the high bandwidth parallel datastream, the control logic routing the high bandwidth parallel datastream to the serializer when the extra packet is not being transmitted **[Fig. 3; Management & Control Block 330, Elastic FIFO 401/Transmit Block 310; namely, no frequency difference between a recovered clock and a local reference clock and thus no insertion or deletion of bytes are required; col. 4, lines 48-65]** and routing the output of the memory holding the extra packet to the serializer while transmitting the extra packet forming the low bandwidth channel **[Fig. 3; Management & Control Block 330, Elastic FIFO 401/Transmit Block 310; namely, there is a frequency difference between a recovered clock and a local reference clock and thus insertion or deletion of bytes are required; col. 4, lines 48-65]**.

Regarding claim 2, Hoang further teaches the control logic uses a state machine memory **[Fig. 3; A state machine is inherent in Hoang in order for Management & Control Block 330 to manage and control the Transmit Block 310 & Receive Block 320]**.

Regarding claim 3, Hoang teaches the memory holding the high bandwidth parallel datastream is organized as a first-in-first-out memory **[Fig. 3; Lane Alignment FIFO 308/Transmit Block 310]**.

Regarding claim 6, Hoang teaches the memory holding the extra packet for the low-bandwidth channel is a portion of the first-in-first-out memory **[Fig. 3; Elastic FIFO 401/Transmit Block 310; col. 4, lines 48-65]**.

Regarding claim 7, Hoang teaches the serializer has an optical output **[Figs. 1 & 3, Optical PMD 30 to Optical Network; PMD 30 acts as an electrical/optical interface; col. 5, lines 42-53]**.

Regarding claim 8, Hoang teaches the serializer has an electrical output **[Figs. 1 & 3; PMD 30 acts as an electrical/optical interface; col. 5, lines 42-53]**.

Regarding claim 9, Hoang teaches a method comprising:

converting the high-bandwidth serial channel to a high bandwidth parallel datastream **[Fig. 3; CDR & Deserializer/Transmit Block 310]**;

holding an extra packet for the low-bandwidth channel in a memory **[Fig. 3; Elastic FIFO 401/Transmit Block 310; col. 4, lines 48-65]**;

capturing the high bandwidth parallel datastream in a memory while the packet for the low bandwidth channel is being sent **[Fig. 3; CMU & Serializer/Transmit Block 310]**; and

selecting under control of a state machine either the high bandwidth parallel datastream or the extra packet in the low bandwidth channel memory for conversion from parallel to serial form **[Fig. 3; Management & Control Block 330, Elastic FIFO 401/Transmit Block 310; namely, there is a frequency difference between a recovered clock and a local reference clock and thus insertion or deletion of bytes are required; col. 4, lines 48-65]**.

Regarding claim 10, Hoang teaches the conversion from parallel to serial form produces an optical output **[Figs. 1 & 3, Optical PMD 30 to Optical Network; PMD 30 acts as an electrical/optical interface; col. 5, lines 42-53]**.

Regarding claim 11, Hoang teaches the conversion from parallel to serial form produces an electrical output **[Figs. 1 & 3; PMD 30 acts as an electrical/optical interface; col. 5, lines 42-53]**.

Allowable Subject Matter

2. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent No. 7,089,485 to Azadet et al. disclose "Simple Link Protocol Providing Low Overhead Coding For LAN Serial And WDM Solutions"
- US Patent No. 7,127,648 to Jiang et al. disclose "System And Method For Performing On-Chip Self-Testing"
- US Patent Application Pub. No. 2004/0156314 A1 by Lund et al. disclose "Method And System For Exploiting Spare Link Bandwidth In A Multilane Communication Channel"

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert T. Chou whose telephone number is 571-272-6045. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Albert T. Chou
May 10, 2007 AC

CHI PHAM
SUPERVISORY PATENT EXAMINER 5/16/07